Serial Number: 10/006,292 Filing Date: December 3, 2001

Title: INTEGRATED CIRCUIT PACKAGE WITH SANDWICHED CAPACITORS (as amended)

Assignee: Intel Corporation

Dkt: 884.534US1 (INTEL)

Page 3

IN THE CLAIMS

Please amend the claims by canceling claims 1-15 and 31-37 and by adding new claims

65-99.

Claims 1-15. (Canceled)

16. (Original) An integrated circuit (IC) package comprising:

a substrate having a plurality of conductors within an IC mounting region;

at least one capacitor within the IC mounting region and electrically coupled to at least

one of the conductors; and

an IC electrically coupled to the plurality of conductors.

17. (Original) The IC package recited in claim 16, wherein the at least one capacitor is

electrically coupled to first and second conductors of the plurality of conductors, and wherein the

first conductor is to couple to a first potential, and the second conductor is to couple to a second

potential.

18. (Original) The IC package recited in claim 16, wherein the at least one capacitor is

mounted atop the at least one conductor.

19. (Original) The IC package recited in claim 18, wherein the at least one capacitor is

mounted atop two conductors.

20. (Original) The IC package recited in claim 18, wherein the at least one capacitor is a

capacitor array having two surfaces, each having a plurality of terminals of first and second

polarity types.

Serial Number: 10/006,292 Filing Date: December 3, 2001

Title: INTEGRATED CIRCUIT PACKAGE WITH SANDWICHED CAPACITORS (as amended)

Assignee: Intel Corporation

21. (Original) The IC package recited in claim 20, wherein the plurality of terminals are

Page 4

Dkt: 884.534US1 (INTEL)

disposed over substantially the entire surfaces.

22. (Original) The IC package recited in claim 16, wherein the at least one capacitor is

mounted beside the at least one conductor.

23. (Original) The IC package recited in claim 16, wherein the at least one capacitor is

mounted between two conductors.

24. (Original) The IC package recited in claim 16, wherein the at least one capacitor has a

top, a bottom, and a pair of opposing sides, and wherein the at least one capacitor is from the

group comprising a capacitor having terminals on its top and bottom, a capacitor having

terminals on its opposing sides, and a capacitor having terminals on its top, bottom, and opposing

sides.

25. (Original) The IC package recited in claim 16, wherein the conductors include at least

one conductive bar having a height and a width, the height exceeding the width, and wherein the

at least one capacitor is mounted beside and in electrical contact with the at least one conductive

bar.

26. (Original) The IC package recited in claim 16, wherein the plurality of conductors are

substantially parallel to one another.

27. (Original) The IC package recited in claim 26, wherein the at least one capacitor is non-

orthogonally mounted atop the at least one conductor.

Page 5 Dkt: 884.534US1 (INTEL)

Serial Number: 10/006,292 Filing Date: December 3, 2001

Title: INTEGRATED CIRCUIT PACKAGE WITH SANDWICHED CAPACITORS (as amended)

Assignee: Intel Corporation

- 28. (Original) The IC package recited in claim 16 and comprising a plurality of capacitors distributed substantially throughout the IC mounting region, each capacitor being in electrical contact with at least one of the conductors.
- 29. (Original) The IC package recited in claim 28, wherein the plurality of capacitors comprises a plurality of sets of capacitors, each set comprising one or more capacitors aligned substantially end-to-end.
- 30. (Original) The IC package recited in claim 16, wherein the conductors include pads.

Claims 31-64 (Canceled)

- 65. (New) An integrated circuit (IC) package comprising:
  - a substrate having a plurality of conductors within an IC mounting region;
- at least one capacitor within the IC mounting region and electrically coupled to at least one of the conductors, wherein the at least one capacitor is mounted atop the at least one conductor; and
  - an IC electrically coupled to the plurality of conductors via the at least one capacitor.
- 66. (New) The IC package recited in claim 65, wherein the at least one capacitor is electrically coupled to first and second conductors of the plurality of conductors, and wherein the first conductor is to couple to a first potential, and the second conductor is to couple to a second potential.
- 67. (New) The IC package recited in claim 65, wherein the at least one capacitor has a top and a bottom, and wherein the at least one capacitor has terminals on its top and bottom.

Serial Number: 10/006,292 Filing Date: December 3, 2001

Title: INTEGRATED CIRCUIT PACKAGE WITH SANDWICHED CAPACITORS (as amended)

Assignee: Intel Corporation

68. (New) The IC package recited in claim 65 and comprising a plurality of capacitors distributed substantially throughout the IC mounting region, each capacitor being in electrical

Page 6

Dkt: 884.534US1 (INTEL)

contact with at least one of the conductors.

69. (New) The IC package recited in claim 68, wherein the plurality of capacitors comprises

a plurality of sets of capacitors, each set comprising two or more capacitors having ends and

being aligned substantially end-to-end.

70. (New) An integrated circuit (IC) package comprising:

a substrate having a plurality of conductors within an IC mounting region;

a plurality of capacitors distributed substantially throughout the IC mounting region and

electrically coupled to at least one of the conductors, wherein the plurality of capacitors

comprises a plurality of capacitor arrays; and

an IC electrically coupled to the plurality of conductors via the plurality of capacitors.

71. (New) The IC package recited in claim 70, wherein selected ones of the plurality of

capacitors are electrically coupled to first and second conductors of the plurality of conductors,

and wherein the first conductor is to couple to a first potential, and the second conductor is to

couple to a second potential.

72. (New) The IC package recited in claim 70, wherein each of the plurality of capacitors has

a top and a bottom, and wherein selected ones of the plurality of capacitors have at least one

terminal on their top and at least one terminal on their bottom.

73. (New) The IC package recited in claim 70, wherein each of the capacitor arrays has a top

and a bottom, and wherein selected ones of the capacitor arrays have a plurality of terminals of

first and second polarities on their top and a plurality of terminals of first and second polarities

on their bottom.

Serial Number: 10/006,292 Filing Date: December 3, 2001

Title: INTEGRATED CIRCUIT PACKAGE WITH SANDWICHED CAPACITORS (as amended)

Assignee: Intel Corporation

Page 7

Dkt: 884.534US1 (INTEL)

74. (New) The IC package recited in claim 70, wherein selected ones of the plurality of

capacitor arrays are interdigitated capacitors.

75. (New) An integrated circuit (IC) package comprising:

a substrate having a plurality of conductors within an IC mounting region, wherein the

plurality of conductors are substantially parallel to one another;

a plurality of capacitors within the IC mounting region and electrically coupled to at least

one of the conductors, wherein the plurality of capacitors comprises a plurality of capacitor

arrays; and

an IC electrically coupled to the plurality of conductors via the plurality of capacitors.

76. (New) The IC package recited in claim 75, wherein selected ones of the plurality of

capacitors are electrically coupled to first and second conductors of the plurality of conductors,

and wherein the first conductor is to couple to a first potential, and the second conductor is to

couple to a second potential.

77. (New) The IC package recited in claim 75, wherein each of the plurality of capacitors has

a top and a bottom, and wherein selected ones of the plurality of capacitors have at least one

terminal on their top and at least one terminal on their bottom.

78. (New) The IC package recited in claim 75, wherein each of the capacitor arrays has a top

and a bottom, and wherein selected ones of the capacitor arrays have a plurality of terminals of

first and second polarities on their top and a plurality of terminals of first and second polarities

on their bottom.

79. (New) The IC package recited in claim 75, wherein the plurality of capacitor arrays are

non-orthogonally mounted atop the plurality of conductors.

Serial Number: 10/006,292

Filing Date: December 3, 2001

Title: INTEGRATED CIRCUIT PACKAGE WITH SANDWICHED CAPACITORS (as amended)

Assignee: Intel Corporation

Dkt: 884.534US1 (INTEL)

80. (New) The IC package recited in claim 79, wherein the conductors are diagonal to the

plurality of capacitor arrays.

81. (New) An integrated circuit (IC) package comprising:

a substrate having a plurality of conductors within an IC mounting region;

a capacitor array within the IC mounting region and electrically coupled to at least one of

the conductors; and

an IC electrically coupled to the plurality of conductors via the capacitor array.

82. (New) The IC package recited in claim 81, wherein the capacitor array is electrically

coupled to first and second conductors of the plurality of conductors, and wherein the first

conductor is to couple to a first potential, and the second conductor is to couple to a second

potential.

83. (New) The IC package recited in claim 81, wherein the capacitor array is non-

orthogonally mounted atop the plurality of conductors.

84. (New) The IC package recited in claim 81, wherein the capacitor array has a top and a

bottom, and wherein the capacitor array has at least one terminal on its top and at least one

terminal on its bottom.

85. (New) The IC package recited in claim 84, wherein the capacitor array has a plurality of

terminals of first and second polarities on its top and a plurality of terminals of first and second

polarities on its bottom.

Serial Number: 10/006,292 Filing Date: December 3, 2001

Title: INTEGRATED CIRCUIT PACKAGE WITH SANDWICHED CAPACITORS (as amended)

Assignee: Intel Corporation

Page 9

Dkt: 884.534US1 (INTEL)

86. (New) The IC package recited in claim 81, wherein the plurality of conductors comprise at least first and second conductive bars having a height and a width, the height exceeding the width, and wherein the first conductive bar is to couple to a first potential, and wherein the second conductive bar is to couple to a second potential.

- 87. (New) The IC package recited in claim 86, wherein the at least first and second conductive bars have a gap to accommodate the capacitor array.
- 88. (New) An integrated circuit (IC) package comprising:

a substrate having a plurality of conductors within an IC mounting region, wherein the conductors include at least one conductive bar having a height and a width, the height exceeding the width;

a plurality of capacitors within the IC mounting region, wherein the plurality of capacitors are mounted beside and in electrical contact with the at least one conductive bar; and an IC electrically coupled to the plurality of conductors via the plurality of capacitors.

- 89. (New) The IC package recited in claim 88, wherein the plurality of conductors comprises at least first and second conductive bars, wherein the first conductive bar is to couple to a first potential, and wherein the second conductive bar is to couple to a second potential.
- 90. (New) The IC package recited in claim 88, wherein selected ones of the plurality of capacitors have a first side and a second side, wherein the first side comprises at least one terminal of first polarity, and wherein the second side comprises at least one terminal of second polarity.
- 91. (New) The IC package recited in claim 88, wherein selected ones of the plurality of capacitors are mounted beside one of the plurality of conductors.

Serial Number: 10/006,292 Filing Date: December 3, 2001

Title: INTEGRATED CIRCUIT PACKAGE WITH SANDWICHED CAPACITORS (as amended)

Assignee: Intel Corporation

92. (New) The IC package recited in claim 88, wherein selected ones of the plurality of

Page 10

Dkt: 884.534US1 (INTEL)

capacitors are mounted between two of the plurality of conductors.

93. (New) The IC package recited in claim 88, wherein the at least one conductive bar has a

length, and wherein at least one of the plurality of capacitors has a length substantially the same

as the length of the at least one conductive bar.

94. (New) The IC package recited in claim 88, wherein the plurality of conductors comprises

at least first and second conductive bars having a height and a width, the height exceeding the

width, wherein the first conductive bar is to couple to a first potential, wherein the second

conductive bar is to couple to a second potential, wherein the first and second conductive bars

have a length, wherein at least one of the plurality of capacitors has a length substantially the

same as the length of the first and second conductive bars and is mounted beside and in electrical

contact with the first and second conductive bars, wherein at least another of the plurality of

capacitors is a capacitor array, and wherein the at least first and second conductive bars have a

gap to accommodate the capacitor array.

95. (New) The IC package recited in claim 94, wherein the capacitor array has a top and a

bottom, wherein the capacitor array has at least one terminal on its top and at least one terminal

on its bottom, and wherein the at least one terminal on its bottom is coupled to one of the first

and second conductive bars.

96. (New) The IC package recited in claim 94, wherein the capacitor array is transverse to

the at least one capacitor.

Serial Number: 10/006,292

Filing Date: December 3, 2001

Title: INTEGRATED CIRCUIT PACKAGE WITH SANDWICHED CAPACITORS (as amended)

Assignee: Intel Corporation

97. (New) An integrated circuit (IC) package comprising:

a substrate having a plurality of conductive bars within an IC mounting region, the conductive bars having a height and a width, the height exceeding the width;

a plurality of capacitors within the IC mounting region, wherein the plurality of capacitors are mounted beside and in electrical contact with selected ones of the conductive bars; and

Page 11

Dkt: 884.534US1 (INTEL)

an IC electrically coupled to the plurality of conductive bars via the plurality of capacitors.

- 98. (New) The IC package recited in claim 97, wherein selected ones of the plurality of capacitors have a first side and a second side, wherein the first side comprises at least one terminal of first polarity, and wherein the second side comprises at least one terminal of second polarity.
- 99. (New) The IC package recited in claim 98, wherein the IC comprises a plurality of pads of first and second polarities, wherein the selected ones of the plurality of capacitors have a top and a bottom, wherein at least one terminal on the top is of a first polarity, wherein at least one terminal on the top is of a second polarity, wherein the at least one terminal of first polarity is coupled to at least one corresponding pad of first polarity, and wherein the at least one terminal of second polarity is coupled to at least one corresponding pad of second polarity.